WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory cell array having a plurality of memory cells arranged in an array from;

a word line driving circuit receiving a constant voltage that does not depend on a provided power supply voltage as a driving voltage and driving a selected word line by the constant voltage; and

a sense amplifier amplifying a high level voltage of a selected bit line to the power supply voltage.

2. The semiconductor memory device according to claim 1, wherein said memory cells is a dynamic random access memory; and wherein a voltage read and amplified by said sense amplifier is written back to one of the memory cells at a time of a refresh.

3. The semiconductor memory device according to claim 1, further comprising a peripheral circuit of said memory cell array including a circuit for generating a signal defining a transition timing of a control signal to said memory cell array and/or a pulse width of the control signal;

said circuit for generating the signal including a delay circuit for delaying the input signal;

said delay circuit having a characteristic in which a delay time thereof decreases more when the provided power supply voltage is low than when the provided power supply voltage is high.

4. The semiconductor memory device according to claim 3, further comprising a circuit for supplying a constant voltage that does not

depend on the power supply voltage as a boosted voltage to be supplied to a control line of said memory cell array.

5. The semiconductor memory device according to claim 3, wherein said peripheral circuit comprises at least one of:

an X decoder for decoding an address signal and activating the selected word line;

a Y switch selector for performing control so that a Y switch for the bit line selected by decoding the address signal is turned on; and

a sense amplifier for amplifying a signal on the bit line; and wherein

said peripheral circuit comprises:

a circuit for generating a signal for controlling at least one of an input signal to said word line driving circuit, a signal for controlling activation of said sense amplifier, and a signal for controlling precharging of the bit line, based on a result of a predetermined logic operation on the input signal and an output signal of said delay circuit.

6. The semiconductor memory device according to claim 3, wherein said memory cell array, said delay circuit, and said peripheral circuit are driven by a relatively low voltage power supply.

7. The semiconductor memory device according to claim 3, wherein said peripheral circuit is driven by the power supply voltage, and wherein said memory cell array and said delay circuit are driven by the lower power supply voltage obtained by stepping down the power supply voltage.

8. The semiconductor memory device according to claim 1, further

comprising:

a reference voltage generating circuit for generating a reference voltage that does not depend on the power supply voltage; and

a booster circuit for generating a constant boosted voltage that does not depend on the power supply voltage based on the reference voltage and outputting the boosted voltage as the constant voltage.

9. The semiconductor memory device according to claim 1, further comprising:

a reference voltage circuit for generating a reference voltage that does not depend on the power supply voltage;

a comparison circuit for comparing the reference voltage with a divided voltage obtained by voltage dividing an output boosted voltage; and

a booster circuit for receiving a result of comparison by said comparison circuit and charging a charge pump and performing voltage boosting when the result of comparison indicates that the divided voltage is smaller than the reference voltage, the boosted voltage that does not depend on the power supply voltage being output from said booster circuit;

the boosted voltage being supplied as a power supply voltage for said word line driving circuit, the boosted voltage being supplied to the selected word line in said memory cell array, the boosted voltage supplied to the word line when the power supply voltage is reduced being kept to be the same as the boosted voltage when the power supply voltage is high, and reduction of an access speed of one of said memory

cells due to reduction of the power supply voltage being suppressed.

10. The semiconductor memory device according to claim 1, wherein the semiconductor memory device further comprises:

a plurality of power systems for supplying the relatively high power supply voltage and the relatively low voltage power supply, said peripheral circuit in said memory cell array being driven by the relatively low voltage power supply;

a circuit for generating a signal for defining a transition timing of a control signal supplied from said peripheral circuit to said memory cell array and/or a pulse width of the control signal including a delay circuit having a characteristic in which a delay time thereof becomes shorter when the supplied power supply voltage is low than when the power supply voltage is high, the delay circuit being driven by the relatively low voltage power supply;

a reference voltage circuit for generating a reference voltage that does not depend on the power supply voltage and used for a boosted voltage to be supplied to said memory cell array; and

a booster circuit for supplying the constant boosted voltage that does not depend on the power supply voltage based on the reference voltage; and

said memory cell array is driven by the relatively low voltage power supply.

11. The semiconductor memory device according to claim 10, wherein said reference voltage circuit and said booster circuit are driven by the relatively low voltage power supply.

12. The semiconductor memory device according to claim 1, further comprising an interface compliant with a static random access memory; wherein said memory cells comprise the dynamic random access memory.

13. The semiconductor memory device according to claim 3, wherein said delay circuit comprises:

at least one circuit unit comprising:

an inverter including:

a first MOS transistor having a source thereof connected to a first power supply; and

a second MOS transistor having a source thereof connected to a second power supply, having a gate thereof connected in common with a gate of said first MOS transistor to an input terminal, and having a drain thereof connected in common with a drain of said first MOS transistor to an output terminal, said second MOS transistor having a different conductivity type from a conductivity type of said first MOS transistor;

a resistor having one terminal thereof connected to said output terminal of said inverter; and

a MOS capacitor connected between the other terminal of said resistor and said first or second power supply.

14. The semiconductor memory device according to claim 13, wherein in said delay circuit, a capacitance value of said MOS capacitor increases when a voltage at said other terminal of said resistor transitions from the power supply voltage of one of said first

and second power supplies to the power supply voltage of the other of said first and second power supplies, one terminal of said MOS capacitor being connected to said other terminal of said resistor and the other terminal of said MOS capacitor being connected to said one of said first and second power supplies.

15. The semiconductor memory device according to claim 13, wherein in said delay circuit, a depletion layer or an inversion layer is formed in said MOS capacitor according to a transition of a voltage at said other terminal of said resistor from the power supply voltage of one of said first and second power supplies to the power supply voltage of the other of said first and second power supplies, said MOS capacitor being connected to said one of said first and second power supplies.

16. The semiconductor memory device according to claim 13, wherein said delay circuit comprises a plurality of stages of said circuit units connected in cascade; wherein

the input signal is supplied to an input terminal of the inverter of the circuit unit in a first one of said stages; wherein

an output signal is taken from a connection point between the MOS capacitor and the other terminal of the resistor, the one terminal of the resistor being connected to the output terminal of the inverter in the circuit unit in a final one of said stages; and wherein

MOS capacitors in said stages of said circuit units adjacent to each other are connected to said first power supply and said second power supply, alternately.

17. The semiconductor memory device according to claim 13, wherein a threshold voltage value of at least one of said first and second MOS transistors in said inverter in said delay circuit is set to be smaller than a threshold value of an ordinary MOS transistor with a same conductivity type as the conductivity type of said at least one of said first and second MOS transistors.

18. The semiconductor memory device according to claim 13, wherein said delay circuit is the delay circuit comprising one or more inverters connected in cascade;

each of said inverters comprising:

a resistor having one terminal thereof connected to the output terminal of said each of said inverters; and

a capacitance element connected between the other terminal of the resistor and a high potential power supply or a low potential power supply; wherein

a capacitance value of said capacitance element increases when a voltage at the other terminal of the resistor transitions from the power supply voltage of one of said high potential and low potential power supplies to the power supply voltage of the other of said high potential and low potential power supplies, one terminal of said capacitance element being connected to the other terminal of the resistor and the other terminal of said capacitance element being connected to said one of said high potential and low potential power supplies.

19. The semiconductor memory device according to claim 13, wherein said delay circuit comprises:

a first inverter receiving the input signal at an input terminal thereof;

a first resistor having one terminal thereof connected to an output terminal of said first inverter;

a first capacitance element having one terminal thereof and the other terminal thereof connected to the other terminal of said first resistor and said first power supply, respectively, a capacitance value of said first capacitance element changing according to a transition of a voltage at said one terminal thereof connected to said other terminal of said first resistor;

a second inverter with an input terminal thereof connected to a connection point between said first resistor and said first capacitance element;

a second resistor having one terminal thereof connected to an output terminal of said second inverter; and

a second capacitance element having one terminal thereof and the other terminal thereof connected to the other terminal of said second resistor and said second power supply, respectively, a capacitance value of said second capacitance element changing according to a transition of a voltage at said one terminal thereof connected to said other terminal of said second resistor; wherein

a connection node between said second resistor and said second capacitance element is an output terminal of a delayed signal, and an in-phase output signal obtained by delaying a transition edge of the input signal is output from said output terminal.

20. The semiconductor memory device according to claim 19, wherein in said delay circuit,

the capacitance value of said first capacitance element increases when the voltage at said one terminal thereof connected to said other terminal of said first resistor transitions from a power supply voltage of said first power supply to a power supply voltage of said second power supply; and

the capacitance value of said second capacitance element increases when the voltage at said one terminal thereof connected to said other terminal of said second resistor transitions from the power supply voltage of said second power supply to the power supply voltage of said first power supply.

21. The semiconductor memory device according to claim 19, wherein said delay circuit further comprises:

a third capacitance element having one terminal thereof and the other terminal thereof connected to said other terminal of said first resistor and said second power supply, respectively, a capacitance value of said third capacitance element changing according to a transition of a voltage at said one terminal thereof connected to said other terminal of said first resistor; and

a fourth capacitance element having one terminal thereof and the other terminal thereof connected to said other terminal of said second resistor and said first power supply, respectively, a capacitance value of said fourth capacitance element changing according to a transition of a voltage at said one terminal thereof connected to said other terminal

of said second resistor.

22. The semiconductor memory device according to claim 21, wherein in said delay circuit,

the capacitance value of said third capacitance element increases when the voltage at said one terminal thereof connected to said other terminal of said first resistor transitions from a power supply voltage of said second power supply to a power supply voltage of said first power supply; and

the capacitance value of said fourth capacitance element increases when the voltage at said one terminal thereof connected to said other terminal of said second resistor transitions from the power supply voltage of said first power supply to the power supply voltage of said second power supply.

23. The semiconductor memory device according to claim 19, wherein in said delay circuit, said first capacitance element comprises a MOS capacitor; the MOS capacitor constituting said first capacitance element changing to an inversion state when the voltage at said other terminal of said first resistor transitions from the power supply voltage of said first power supply to the power supply voltage of said second power supply; and said second capacitance element comprises a MOS capacitor; the MOS capacitor constituting said second capacitance element changing to an inversion state when the voltage at said other terminal of said second resistor transitions from the power supply voltage of said second power supply to the power supply voltage of said first power supply.

24. The semiconductor memory device according to claim 21, wherein in said delay circuit, said third capacitance element comprises a MOS capacitor; the MOS capacitor constituting said third capacitance element changing to an inversion state when the voltage at said other terminal of said first resistor transitions from the power supply voltage of said second power supply to the power supply voltage of said first power supply; and said fourth capacitance element comprises a MOS capacitor; the MOS capacitor constituting said fourth capacitance element changing to an inversion state when the voltage at said other terminal of said second resistor transitions from the power supply voltage of said first power supply to the power supply voltage of said second power supply.

25. The semiconductor memory device according to claim 19, wherein said delay circuit further comprise

a reset circuit having a first switch inserted between said first power supply and said other terminal of said first resistor, said first switch having a control terminal thereof connected to said input terminal of said first inverter.

26. The semiconductor memory device according to claim 19, wherein said delay circuit further comprises

a reset circuit comprising:

a third inverter having an input terminal thereof connected to said input terminal of said first inverter; and

a second switch inserted between said other terminal of said second resistor and said second power supply; said second switch

having a control terminal thereof connected to an output terminal of said third inverter.

27. The semiconductor memory device according to claim 21, wherein said delay circuit further comprises:

a third switch inserted between said first power supply and a power supply terminal of said first inverter, for being controlled to turn on when a control signal for reset indicates a first logic value;

a fourth switch inserted between said output terminal of said first inverter and said second power supply, for being controlled to turn on when said control signal indicates a second logic value; and

a fifth switch inserted between a power supply terminal of said second inverter and said second power supply, for being controlled to turn on when said control signal indicates said first logic value.

28. The semiconductor memory device according to claim 3, wherein said delay circuit comprises

a first inverter comprising:

a first MOS transistor of a first conductivity type having a source thereof connected to a first power supply; and

a second MOS transistor of a second conductivity type, having a source thereof connected to a second power supply, having a gate thereof connected in common with a gate of said first MOS transistor to an input terminal, and having a drain thereof connected in common with a drain of said first MOS transistor to an output terminal;

a first resistor having one terminal thereof connected to said output terminal of said first inverter;

a first capacitance comprising a MOS capacitor of said first conductivity type; said first capacitance being connected between the other terminal of said first resistor and said first power supply;

a second inverter comprising:

a third MOS transistor of said first conductivity type having a source thereof connected to said first power supply; and

a fourth MOS transistor of said second conductivity type, having a source thereof connected to said second power supply, having a gate thereof connected in common with a gate of said third MOS transistor to an input terminal, and having a drain thereof connected in common with a drain of said first MOS transistor to an output terminal; a connection node between said first resistor and said first capacitance being connected to said input terminal of said second inverter;

a second resistor having one terminal thereof connected to said output terminal of said second inverter; and

a second capacitance comprising a MOS capacitor of said second conductivity type, said second capacitance being connected between the other terminal of said second resistor and said second power supply; wherein

said input terminal of said first inverter is a signal input terminal, and a connection node between said second resistor and said second capacitance is a signal output terminal.

29. The semiconductor memory device according to claim 28, wherein said delay circuit further comprises:

a MOS transistor of said first conductivity type having a gate

thereof connected to said input terminal of said first inverter, having a source thereof connected to said first power supply, and having a drain thereof connected to said other terminal of said first resistor.

30. The semiconductor memory device according to claim 28, wherein said delay circuit further comprises:

a third inverter having an input terminal thereof connected to said input terminal of said first inverter; and

a MOS transistor of said second conductivity type, having a gate thereof connected to an output terminal of said third inverter, having a source thereof connected to said second power supply, and having a drain thereof connected to said other terminal of said second resistor.

31. The semiconductor memory device according to claim 3, wherein said delay circuit comprises:

a first inverter comprising:

a first MOS transistor of a first conductivity type having a source thereof connected to a first power supply; and

a second MOS transistor of a second conductivity type, having a source thereof connected to a second power supply, having a gate thereof connected in common with a gate of said first MOS transistor to an input terminal, and having a drain thereof connected in common with a drain of said first MOS transistor to an output terminal;

a first resistor having one terminal thereof connected to said output terminal of said first inverter;

a first capacitance comprising a MOS capacitor of said first conductivity type, said first capacitance being connected between the

other terminal of said first resistor and said first power supply;

a second inverter comprising:

a third MOS transistor of said first conductivity type having a source thereof connected to said first power supply; and

a fourth MOS transistor of said second conductivity type, having a source thereof connected to said second power supply, having a gate thereof connected in common with a gate of said third MOS transistor to an input terminal, and having a drain thereof connected in common with a drain of said third MOS transistor to an output terminal,

a connection point between said first resistor and said first capacitance being connected to said input terminal of said second inverter;

a second resistor having one terminal thereof connected to said output terminal of said second inverter;

a second capacitance comprising a MOS capacitor of said second conductivity type, said second capacitance being connected between the other terminal of said second resistor and said second power supply,

said input terminal of said first inverter being a signal input terminal, and a connection point between said second resistor and said second capacitance being a signal output terminal;

a third capacitance comprising the MOS capacitor of said second conductivity type, said third capacitance being connected between said other terminal of said first resistor and said second power supply; and

a fourth capacitance comprising the MOS capacitor of said first conductivity type, said fourth capacitance being connected between

said other terminal of said second resistor and said first power supply.

32. The semiconductor memory device according to claim 31, wherein said delay circuit comprises:

a first switch comprising MOS transistor of said first conductivity type, having a source thereof and a drain thereof connected to said first power supply and said source of said first MOS transistor of said first inverter, respectively, and having a gate thereof for receiving a control signal for reset;

a second switch comprising a MOS transistor of said second conductivity type, having a source thereof and a drain thereof connected to said output terminal of said first inverter and said second power supply, respectively, and having a gate thereof for receiving the control signal for reset; and

a third switch comprising a MOS transistor of said second conductivity type, having a source thereof and a drain thereof connected to said source of said fourth MOS transistor of said second inverter and said second power supply, respectively, and having a gate thereof for receiving the control signal for reset.

33. The semiconductor memory device according to claim 28, wherein in said delay circuit, threshold values of said second MOS transistor and said third MOS transistor are set to be lower than threshold values of ordinary MOS transistors of said second conductivity type and said first conductivity type, respectively.

34. The semiconductor memory device according to claim 13, wherein in said delay circuit, said resistor comprises a diffusion

resistance on a substrate.

35. The semiconductor memory device according to claim 19, wherein in said delay circuit, each of said first resistor and said second resistor comprises a diffusion resistance on a substrate.

36. The semiconductor memory device according to claim 19, wherein a power supply voltage of one of said first and second power supplies being at a higher potential is used as the power supply voltage stepped down by a voltage step-down circuit for stepping down the power supply voltage.

37. The semiconductor memory device according to claim 3, wherein at least said delay circuit is driven by the relatively low voltage power supply; and wherein

other circuits formed on a same chip as said delay circuit are driven by the relatively high power supply voltage or the relatively low voltage power supply.

38. A semiconductor device comprising the delay circuit according to claim 13, as a delay circuit having a characteristic in which a delay time thereof decreases more when a provided power supply voltage is low than when the provided power supply voltage is high.

39. A semiconductor device comprising:

a delay circuit for delaying an input signal and outputting a so delayed signal; and

a circuit for outputting a result of a predetermined logic operation on the input signal and an output signal of said delay circuit;

wherein the semiconductor device comprises the delay circuit

according to claim 13 as said delay circuit.

40. The semiconductor memory device according to claim 3, wherein the constant voltage is constant irrespective of the power supply voltage at a time of low voltage driving which uses the relatively low voltage power supply and a delay time of the control signal at the time of the low voltage driving decreases more than at a time of high voltage driving which uses the relatively high power supply voltage, due to said characteristic of said delay circuit, an access time of said memory cell array decreases more at the time of the low voltage driving than at the time of the high voltage driving, and the decrease in the access time of said memory cell array at the time of the low voltage driving from the access time at the time of the high voltage driving cancels out at least part of an increase in an access time caused by reduction of an operation speed of said peripheral circuit of said memory cell array due to the low voltage driving, so that an increase in a delay of an overall access time of said memory cell array and said peripheral circuit at the time of the low voltage driving is suppressed.

41. A method of controlling a semiconductor memory device comprising a memory cell array having a plurality of memory cells arranged in an array form, a word line driving circuit for selecting a word line of said memory cell array, and a sense amplifier connected to bit lines, said method comprising the steps of:

generating a constant voltage that does not depend on a provided power supply voltage;

receiving by said word line driving circuit the generated

constant voltage as a driving voltage for driving a selected word line by the constant voltage; and

amplifying by said sense amplifier a higher voltage level of a selected bit line to the power supply voltage.

42. The method according to claim 41, further comprising the step of:

delaying an input signal by a delay circuit when a peripheral circuit for said memory cell array generates a signal for defining a transition timing and/or a pulse width of the control signal to said memory cell array;

wherein said delay circuit has a characteristic in which a delay time thereof decreases more when the provided power supply voltage is lower than when the provided power supply voltage is higher.

43. The method according to claim 42, wherein said memory cell array, said delay circuit, and said peripheral circuit are driven by the relatively low voltage power supply.

44. The method according to claim 42, wherein said peripheral circuit is driven by the power supply voltage, and said memory cell array and said delay circuit are driven by the low voltage power supply obtained by stepping down the power supply voltage.

45. The method according to claim 41, further comprising the steps of:

driving said memory cell array and a peripheral circuit thereof by the relatively low voltage power supply;

supplying a constant voltage that does not depend on the power

supply voltage as a boosted voltage to be supplied to a control signal for said memory cell array; and

performing signal delay using a delay circuit having a characteristic in which a delay time thereof decreases with reduction of the power supply voltage, by a circuit for generating the signal for defining a transition timing and/or a pulse width of the control signal supplied from said peripheral circuit to said memory cell array.

46. The method according to claim 41, further comprising the steps of:

performing signal delay using a delay circuit having a reverse characteristic in which a delay time thereof decreases with reduction of the power supply voltage, by a circuit for generating a signal for defining a transition timing and/or a pulse width of a control signal supplied from a peripheral circuit of said memory cell array to said memory cell array;

driving said peripheral circuit by the power supply voltage;

driving said delay circuit by a stepped-down power supply voltage obtained by stepping down the power supply voltage;

supplying the constant voltage that does not depend on rise and fall of the power supply voltage as a boosted voltage to be supplied to a control signal for said memory cell array; and

driving said memory cell array by the stepped-down power supply voltage obtained by stepping down the power supply voltage.

47. The method according to claim 42, wherein when a transition edge of a logic signal is delayed by said delay circuit comprising one

or more inverters connected in cascade, one terminal of a resistor is connected to an output terminal of each of said one or more inverters, and the other terminal of said resistor is connected to a power supply through a MOS capacitor; and wherein

said method comprises:

(a) a step of the inverter receiving at an input terminal thereof a rising or falling transition signal from an input terminal or from the other terminal of the resistor having one terminal thereof connected to the output terminal of the inverter at a preceding stage; and

(b) a step of the MOS capacitor being changed to an inversion state when an output signal of said inverter transitions from one logic value to the other logic value, said one logic value corresponding to said power supply with the MOS capacitor connected thereto, the MOS capacitor corresponding to said each of said one or more inverters to which the transition signal is supplied.

48. The method of controlling a semiconductor memory device according to claim 42, wherein

since the constant voltage is constant irrespective of the power supply voltage at a time of low voltage driving using the relatively low voltage power supply and a delay time of the control signal decreases more at the time of the low voltage driving than at a time of high voltage driving using the relatively high power supply voltage due to said characteristic of said delay circuit, an access time of said memory cell array decreases more at the time of the low voltage driving than at the time of the high voltage driving; and wherein

control is so performed that the decrease of the access time at the time of the low voltage driving from the access time at the time of the high voltage driving cancels out at least part of an increase in an access time caused by reduction of an operation speed of said peripheral circuit of said memory cell array due to the low voltage driving, and an increase in a delay of an overall access time of said memory cell array and said peripheral circuit at the time of the low voltage driving is suppressed.

49. A memory device, comprising:

a memory cell array including a plurality of memory cells;

a driver for driving a word line coupled to the selected memory cell;

a first control circuit for generating a control signal to control said driver; and

a sense amplifier for amplifying a voltage on a bit line coupled to the selected memory cell;

wherein said first control circuit has a first delay characteristic in which the higher a power supply voltage applied to the first control circuit becomes, the larger a delay time of the first control circuit becomes, while said sense amplifier has a second delay characteristic in which the higher a power supply voltage applied to said sense amplifier becomes, the smaller a delay time of the circuit becomes.

50. A memory device, comprising:

a memory cell array including a plurality of memory cells; and

a first control circuit for accessing a selected memory cell;

said first control circuit having a first delay characteristic in which the higher a power supply voltage applied to the first control circuit becomes, the larger a delay time of the first control circuit becomes.

51. The memory device according to claim 50, further comprising

a second control circuit for accessing the selected memory cell;

said second control circuit having a second delay characteristic in which the higher a power supply voltage applied to the second control circuit becomes, the smaller a delay time of the second control circuit becomes.